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WHAT IS CLAIMED IS:

1. An ESD protection structure for use with an integrated circuit comprising:

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type disposed in the semiconductor substrate;

a second well region of the second conductivity type disposed in the semiconductor

a gap region of the first conductivity type disposed in the semiconductor substrate and separating the first well region from the second well region,

a first floating region of the second conductivity type disposed in the first well region adjacent to the gap region;

a second floating region of the second conductivity type disposed in the second well region adjacent to the gap region;

a first contact region of the first conductivity type disposed on the first well region and spaced apart from the first floating region;

a second contact region of the first conductivity type disposed on the second well region and spaced apart from the second floating region;

a first contact region of the second conductivity type disposed on the first well region and spaced apart from the first floating region;

a second contact region of the second conductivity type disposed on the second well region and spaced apart from the second floating region.

2. The ESD protection structure of claim 1 further comprising:

a first electrical contact connected to the first contact region of the first conductivity type, the first contact region of the second conductivity type, and the integrated circuit; and

a second electrical contact connected to the second contact region of the first conductivity type, the second contact region of the second conductivity type and to ground.

3. The ESD protection structure of claim 1, wherein the first conductivity type is P-type and the second conductivity type is N-type.

4. The ESD protection structure of claim 1, wherein the dopant concentrations of the first floating region and the second floating region are greater than the dopant concentrations of the first well region and the second well region.

5. The ESD protection structure of claim 4, wherein the dopant concentration of the first well region and the second well region is at least 1E17 atoms per cm^2.

6. The ESD protection structure of claim 1, wherein the gap region separates the first well region from the second well region with a minimum distance in the range of 0.18 microns to 0.25 microns.

7. The ESD protection structure of claim 1, wherein the first well region and the second well region are disposed in the semiconductor substrate in an elongated finger configuration.

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